USN | | | | | | | | | | |

06ES32

Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. What do you understand by 'reverse recovery time' of a diode? Explain. **(05 Marks)**

b. The input voltage V_i to the two level clipper circuit [as shown in Fig. Q1(b)] varies linearly from o to 150 V. Sketch the output voltage V_0 to the time scale. Assume diodes as ideal.

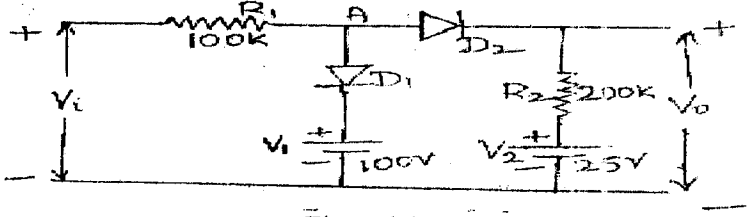


Fig. Q1(b) **(10 Marks)**

c. Draw and explain the working of the clamper circuit which clamps the positive peak of a signal to zero volts. **(05 Marks)**

2 a. Explain the circuit of a transistor switch being used as an inverter. **(05 Marks)**

b. Derive an expression for the stability factor, S(Ico), of the voltage divider Bias circuit. **(06 Marks)**

c. In the circuit of Fig. Q2(c) V_{CC} = 10 V, R_C = 1.5 kΩ, I_C = 2 mA, V_{CE} = 5 V, V_{BE} = 0.7V, β = 50 and stability factor S = 5, find R_1 and R_2.

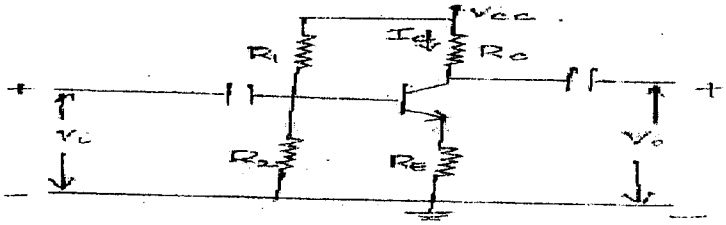


Fig. Q2(c) **(09 Marks)**

3 a. Derive the expressions for A_V, A_I, Z_i and Z_o for CE fixed bias configuration using complete hybrid equivalent model. **(12 Marks)**

b. For common base amplifier shown in Fig Q3(b), determine Z_i, A_I, A_V and Z_o using complete hybrid equivalent model.

Given h_{ie} = 1.6kΩ, h_{fe} = 110

$h_{re} = 2 \times 10^{-4}$, h_{oe} = 20 μS. **(08 Marks)**

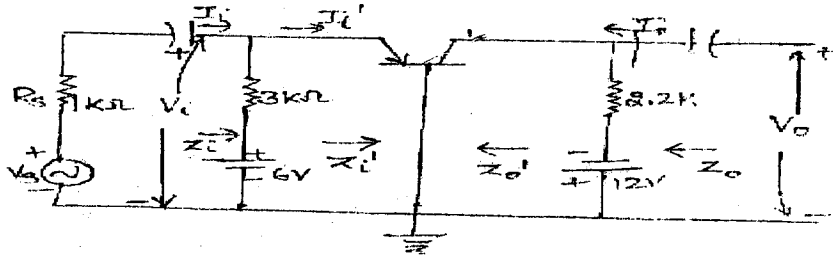


Fig. Q3(b)

4 a. The input power to a device is 10,000 W at a voltage of 1000 V. The out put power is 500W and the output impedance is 20Ω.

i) Find power gain in decibels, ii) Find voltage gain in decibels. **(04 Marks)**

b. Describe miller effect and derive an equation for miller input and output capacitances.

c. Discuss the factors that affect the low frequency response of a BJT–CE amplifier. **(10 Marks)**

5 a. Fig. Q5(a) shows cascading of an emitter follower circuit and a common base circuit. Find
i) The loaded gain of each stage
ii) The total gain for the system, A_V and A_{VS}.
iii) The total current gain for the system
iv) The total gain far the system if the emitter follower circuit were removed. (09 Marks)

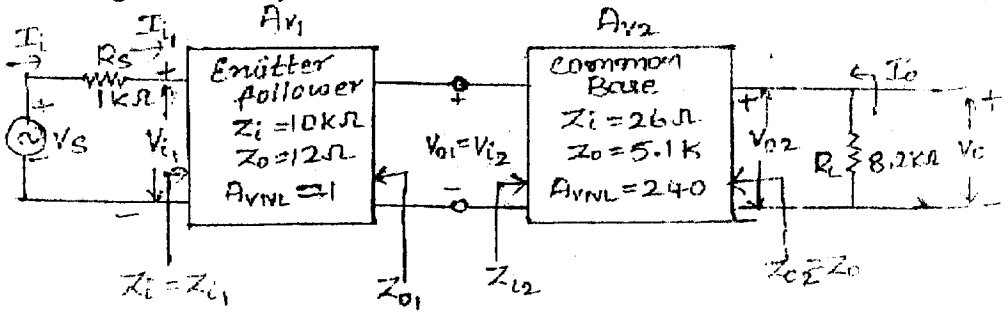


Fig. Q5(a)

b. Show that negative feedback increases the bandwidth of an amplifier. (06 Marks)
c. Derive an expression for output resistance of a voltage series feedback amplifier. (05 Marks)

6 a. With the help of a circuit diagram, explain the working of class–B pushpull amplifier Obtain an expression for maximum conversion efficiency of this amplifier. (09 Marks)
b. Discuss the different types of power amplifiers. (05 Marks)
c. For distortion readings of $D_2 = 0.15$, $D_3 = 0.01$ and $D_1 = 0.05$ with $I_1 = 3.3$ Amps and $R_C = 4\Omega$. Find – i) Total harmonic distortion D, ii) Fundamental power component. iii) Total power. (06 Marks

7 a. What is Barkhausen criterion? Explain how oscillations start in an oscillator. (07 Marks)
b. With the help of a neat circuit diagram, explain transistor colpitts oscillator. Write the expression for the frequency of oscillation. (08 Marks)

c. A quartz crystal has L = 0.12 H, C = 0.04 pF C_M = pF and R = 9.2 kΩ. Find
i) Series resonant frequency, ii) Parallel resonant frequency. (05 Marks)

8 a. Discuss the differences between FET and BJT. (04 Marks)
b. Derive the expressions for Z_i, Z_o and A_V for common drain JFET amplifier. (09 Marks)
c. A dc analysis of source follower network shown in Fig. Q8(c) results in V_{GSQ} = -2.86 V and I_{DQ} = 4.56 mA. Determine
i) g_m, ii) r_d, ii) Z_i, iv) Z_o with and without r_d, v) A_V with and without r_d.
I_{DSS} = 16mA, V_P = -4V, Y_{OS} = 25 μS.

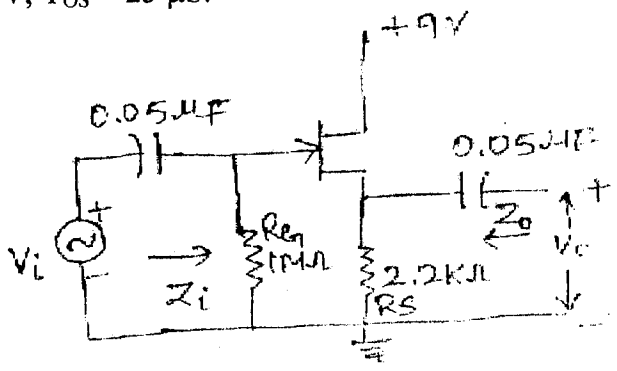


Fig. Q8(c) (07 Marks)

*****

USN | | | | | | | | | | |

06ES32

Third Semester B.E. Degree Examination, June / July 08
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions, selecting atleast two questions from each part.***

PART A

1 a. Differentiate between static and dynamic resistance of a semi conductor diode. **(04 Marks)**

b. Explain with the help of a circuit diagram the working of a Full Wave Rectifier. Derive expressions for i) I_{dc} ii) I_{rms} iii) V_{dc} iv) Ripple factor v) Rectifier efficiency. **(10 Marks)**

c. For the circuit shown, in Fig.Q1(c) write the transfer characteristic equations. Assume diodes are ideal. Plot V_0 against V_i, indicating all slopes and voltage levels. **(06 Marks)**

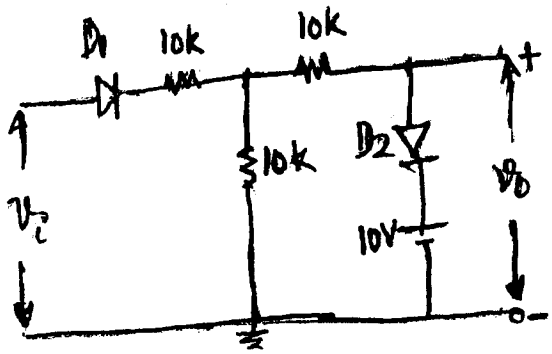


Fig.Q1(c)

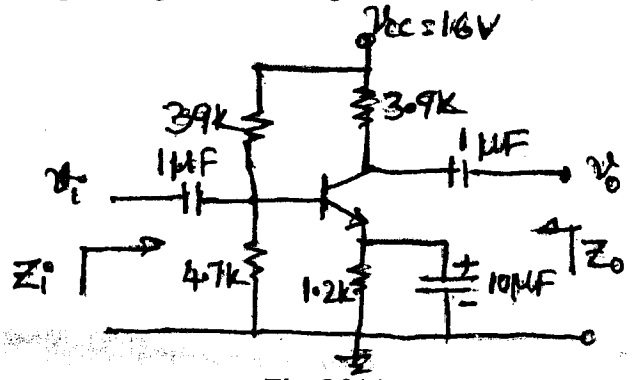


Fig.Q3(a)

2 a. Design a voltage divider bias circuit with V_{CC} = 10 V, R_C = 1.5 K ohm, I_C = 2 mA, V_{CE} = 5 V, β = 50. Assume silicon transistor and stability factor S = 5. **(08 Marks)**

b. Derive an expression for the stability factor $S(I_{CO})$ for a voltage divider bias circuit. **(08 Marks)**

c. Determine R_B and R_C for the transistor inverter of Fig.Q2(c) if I_{Csat} = 10 mA. **(04 Marks)**

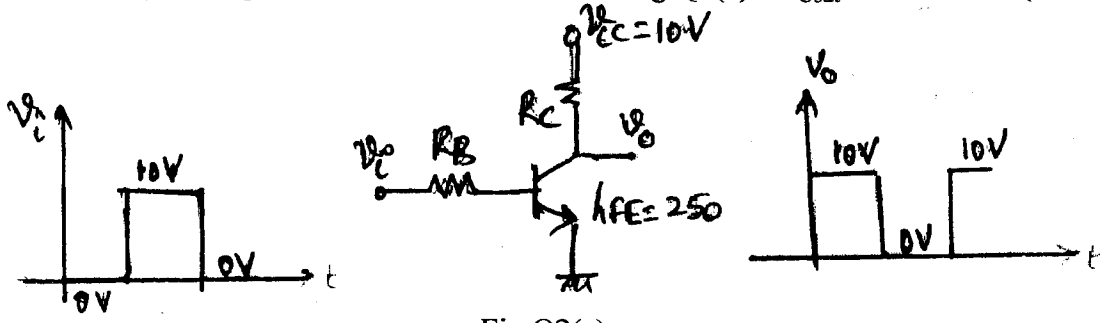


Fig.Q2(c)

3 a. For the network of Fig.Q3(a): i) Determine r_e ii) Calculate Z_i and Z_0 iii) Find A_V Given β = 100 S_i transistor. **(08 Marks)**

b. Draw the emitter follower circuit. Derive expressions for:
i) Z_i ii) Z_0 iii) A_V using r_e model. **(08 Marks)**

c. Define h-parameters. Draw the h-parameter model of a transistor. **(04 Marks)**

4 a. Determine the lower cutoff frequency for the network of Fig.Q4(a). Given β = 100, $r_0 = \infty$ ohm. Determine the mid band gain. If C_{be} = 36 pF, C_{bc} = 4 pF, C_{w_i} = 6 pF, C_{w_0} = 8 pF. Determine f_{H_i} and f_{H_0} and sketch the frequency response for low and high frequency regions using the results. **(12 Marks)**

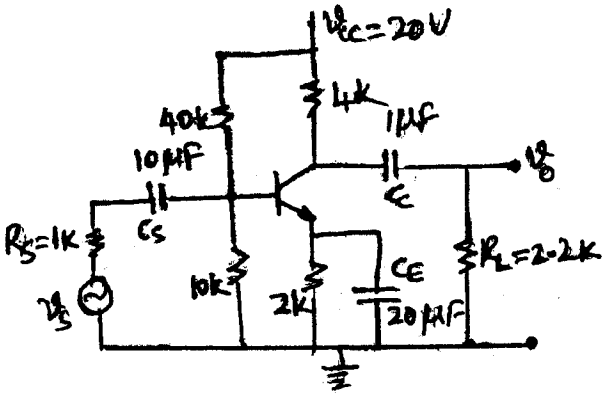


Fig.Q4(a)

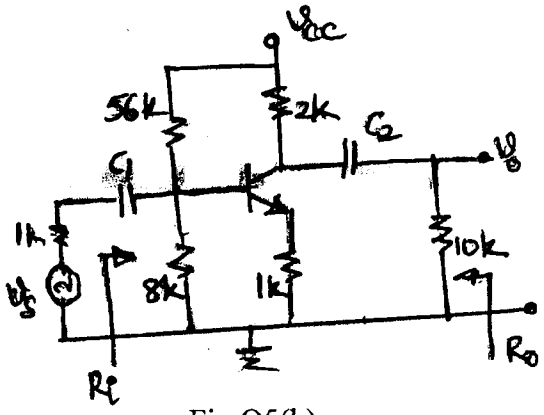


Fig.Q5(b)

b. Calculate the overall lower 3 db and upper 3 db frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(08 Marks)**

PART B

5 a. Draw the cascade configuration and list the advantages of this circuit. **(04 Marks)**

b. Determine A_i, R_i, A_v and R_0 for the circuit shown in fig.Q5(b). Given h parameters $h_{ie} = 1.1$ k ohm, $h_{re} = 2 \times 10^{-4}$, $h_{oe} = 25 \times 10^{-6}$ ℧, $h_{fe} = 50$. **(08 Marks)**

c. List the advantages of negative feedback amplifier. Derive expressions for Z_{if} and Z_{of} for voltage series feedback amplifier. **(08 Marks)**

6 a. Explain the working of a class B push pull amplifier. Prove that the maximum efficiency is 78.5%. **(10 Marks)**

b. A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as $B_0 = 1.5$ mA, $B_1 = 120$ mA, $B_2 = 10$ mA, $B_3 = 4$ mA, $B_4 = 2$ mA, $B_5 = 1$ mA. i) Determine the percentage total harmonic distortion

ii) Assume second identical transistor is used along with suitable transformer to provide push pull operation. Using the above harmonic amplitudes, determine the new total harmonic distortion. **(10 Marks)**

7 a. Explain with the help of a circuit diagram, the working of an RC phase shift oscillator. **(08 Marks)**

b. With the help of Barkhousen criterion, explain the working of a BJT crystal oscillator. **(08 Marks)**

Calculate the frequency of a Wien Bridge oscillator circuit when R = 12 k ohm and C = 2400 pf. **(04 Marks)**

8 a. Determine Z_i, Z_0 and A_v for the circuit shown in Fig.Q8(a), if $Y_{fs} = 3000$ μs and $Y_{os} = 50$ μs. **(06 Marks)**

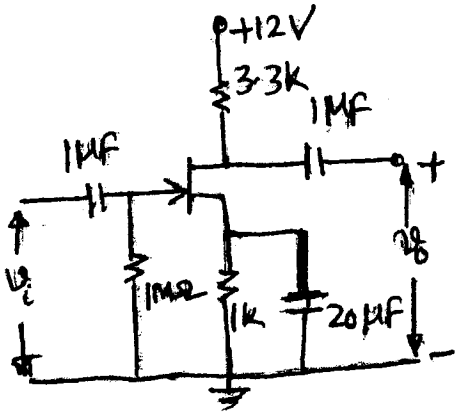


Fig.Q8(a)

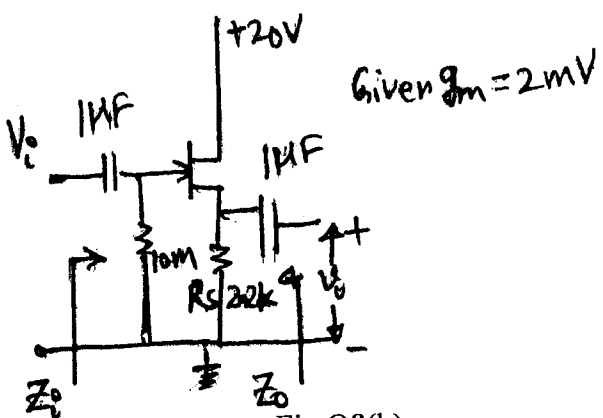


Fig.Q8(b)

b. Determine Z_i, Z_0, and A_v if $r_d = 40$ kΩ for fig.Q8(b). **(06 Marks)**

c. With the help of circuits and equations, show different biasing arrangements for depletion type MOSFET. **(08 Marks)**

*****

USN | | | | | | | | | | |

06ES32

Third Semester B.E. Degree Examination, Dec.08/Jan.09
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***1. Answer any FIVE full questions selecting at least 2 questions from each part.***
2. Draw equivalent circuit wherever necessary.

PART - A

1 a. Explain the different diode equivalent circuits with necessary approximations if any. **(06 Marks)**

b. Explain junction capacitance with reference to a PN – diode. **(06 Marks)**

c. Sketch the waveform of V_0 for the circuit below. **(08 Marks)**

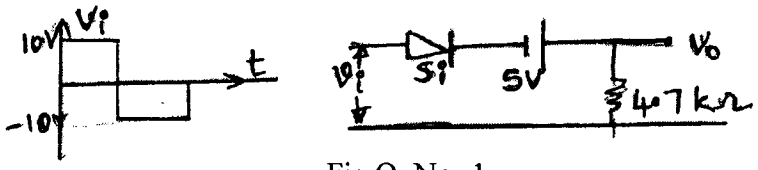


Fig Q. No. 1c.

2 a. Explain with help of load line the effect of variation of V_{CC}, I_B on Q-pt of a transistor. **(06 Marks)**

b. For the voltage Feedback network below determine I_C, V_{CE}, V_C, V_E. **(08 Marks)**

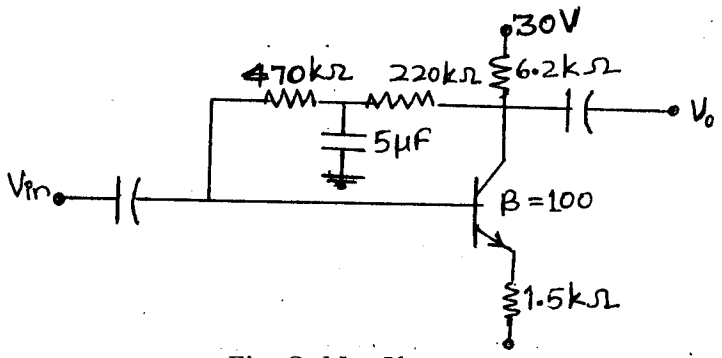


Fig. Q. No. 2b

c. Derive expression for S_{ICO} for a Voltage Divider bias circuit. **(06 Marks)**

3 a. Draw r_e and h – parameter models of a transistor in CE – mode. Give relation between r_e parameters and h – parameters. **(05 Marks)**

b. A voltage divider biased amplifier has $V_{CC} = 20V$, $R_1 = 220k\Omega$, $R_2 = 56k\Omega$, $R_C = 6.8k\Omega$, $R_E = 2.2k\Omega$. The Silicon transistor used has $\beta = 180$ and $r_o = 70k\Omega$.
Find: i) ac emitter diode resistance, re.
ii) Input impedance.
iii) Voltage Gain. Draw the r_e-model equivalent circuit. **(10 Marks)**

c. Given a packaged amplifier below, find
   i) Voltage gain with $R_L = 4k\Omega$.
   ii) Voltage gain with $R_L = 22k\Omega$.
   Comment on the result of Part (i) and (ii) (05 Marks)

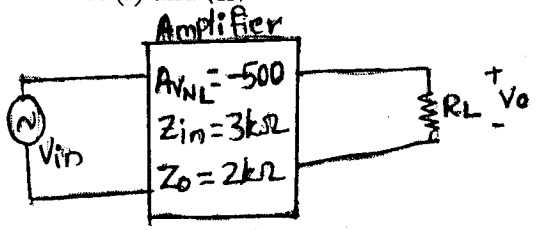


Fig. Q.No. 3c.

4 a. Explain low frequency response of BJT amplifier and give expression for lower cut-off frequency due to C_C, C_E and C_S. (10 Marks)
   b. Obtain expression for miller effect input and miller effect output capacitance. (10 Marks)

PART - B

5 a. With necessary equivalent diagram obtain the expression for Z_{in}, A_v, Z_o for a Darlington Emitter follower. (08 Marks)
   b. What are the effects of negative feedback? (06 Marks)
   c. Obtain expression for Z_{in}, Z_o for a voltage – series feedback. (06 Marks)

6 a. What are the classification of Power Amplifiers based on the location of Q-pt? Also indicate the operating cycle in each case. (06 Marks)
   b. Prove that the maximum conversion efficiency in class-B power amplifier is 78.5%. (08 Marks)
   c. A power amplifier has harmonic distortions $D_2 = 0.1$, $D_3 = 0.02$, $D_4 = 0.01$, the fundamental current $I_1 = 4A$ and $R_L = 8\Omega$. Calculate the total harmonic distortion, fundamental power and total power. (06 Marks)

7 a. Explain characteristics of a quartz crystal. With a neat diagram explain the crystal oscillator in Parallel – resonant circuits. (10 Marks)
   b. Explain how a feedback circuit can be used as oscillator. (04 Marks)
   c. Calculate operating frequency of a BJT phase – Shift oscillator for $R = 6k\Omega$, $C = 1500pF$, $R_C = 18k\Omega$. Determine minimum current gain of transistor required for sustained oscillations. (06 Marks)

8 a. Define transconductance g_m. Derive expression for g_m. (06 Marks)
   b. A JFET has $g_m = 6mV$ at $V_{GS} = -1V$. Find I_{DSS} if pintch off voltage $V_P = -2.5V$. (04 Marks)
   c. With necessary equivalent circuit obtain the expression for A_v, Z_{in}, Z_o for a fixed-biased JFET Amplifier. (10 Marks)

*****

USN | | | | | | | | | | |

06ES32

Third Semester B.E. Degree Examination, June-July 2009
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting at least Two questions from each part.*
2. Make suitable assumptions if necessary.

PART - A

1 a. With respect to a semiconductor diode, explain the following:
i) Reverse Recovery time
ii) Diffusion capacitance. **(06 Marks)**

b. How does a clamping circuit differ from a clipping circuit? For the diode clipping circuit shown in Fig.1(b), draw the input and output waveforms for i) R = 100 Ω; ii) R = 1kΩ; iii) R = 10kΩ for V_i = 20 Sinwt and V_R = 10V. Assume Rf = 100Ω, Rr = ∞ and V_r = 0. **(08 Marks)**

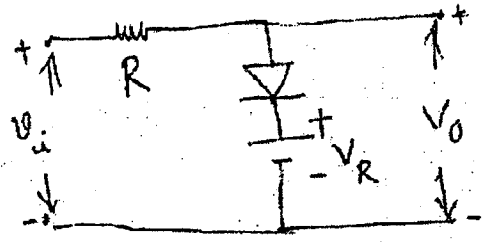


Fig.1(b).

c. Draw the circuit diagram of a full wave rectifier with capacitor filter. The circuit uses a capacitor of 1000 μF and provides a d.c. load current of 500 mA at 2% ripple. Assume f = 50Hz. Calculate i) D.C. output voltage; ii) Peak rectified voltage and % regulation. **(06 Marks)**

2 a. What is meant by transistor biasing? Compare different biasing methods used for transistor biasing with respect to stability. **(05 Marks)**

b. Find the operating point for the voltage divider bias circuit with β = 80 and V_{BE} = 0.6V. Find the new operating point when β changes to 100 and V_{BE} changes to 0.25. Given V_{cc} = 15V, R_1 = 100kΩ, R_2 = 18kΩ, R_c = 4.7kΩ, R_E = 1kΩ. **(07 Marks)**

c. With the help of a neat circuit diagram, explain the use of transistor as an inverter. **(08 Marks)**

3 a. What are the advantages of using hybrid model to represent the transistor? Explain how h-parameters can be obtained from the static characteristics of the transistor. **(06 Marks)**

b. For the Emitter follower circuit, derive expressions for A_V, A_I, R_{in} and R_o of an emitter follower. **(08 Marks)**

c. Compare the characteristics of CE, CC, CB configurations. A CE amplifier uses R_L = 200Ω. The h-parameters are h_{ie} = 1100Ω, h_{re} = 2.5 x 10^{-4}, h_{fe} = 50 and h_{oe} = 22 μA/V. Calculate i) Current gain; ii) Input impedance **(06 Marks)**

4 a. What is Miller effect? Draw the high frequency transistor a.c. equivalent circuit (π-Model) and explain the significance of each component in the model. **(08 Marks)**

b. What are the factors that influence the low frequency and high frequency response of a CE – BJT amplifier? **(06 Marks)**

c. Calculate the overall lower 3dB and upper 3dB frequencies for a 3 stage amplifier having an individual lower 3dB frequency of 30 Hz and upper 3dB frequency of 2.5 MHz. **(06 Marks)**

5 a. Why do we cascade amplifiers? State the various methods of cascading transistor amplifiers. A given amplifier arrangement has the following voltage gains. $Av_1 = 10$. $Av_2 = 20$ and $Av_3 = 40$. What is the overall voltage gain? Also express each gain in dB and determine the total voltage gain in dB. (08 Marks)

b. Explain the operation and characteristics of cascade and Darlington pair connections. (04 Marks)

c. Explain the concept of feedback amplifier. If an amplifier has a bandwidth of 200 kHz and a voltage gain of 80, what will be the new bandwidth and gain if a negative feedback of 5% is introduced? (08 Marks)

6 a. How are power amplifier classified? Explain. Show that the transformer coupled class A amplifier has a maximum efficiency of 50%. (08 Marks)

b. With circuit diagram, explain the working of class B push pull amplifier. Obtain an expression for the maximum conversion efficiency. (07 Marks)

c. What is harmonic distortion? A transistor supplies 0.85 Watts to a 4kΩ load. The zero signal d.c. collector current is 31 mA and the d.c. collector current with signal is 34 mA. Determine the percentage second harmonic distortion. (05 Marks)

7 a. State Barkhausen criteria for sustained oscillations and apply this to R.C phase shift oscillator and explain. Write the expression for the frequency of oscillation. Design the R.C. elements of a weinbridge oscillator for operation at $f_o = 10$kHz. (08 Marks)

b. With the help of a circuit diagram, explain the working of Hartely oscillator. A colpitt's oscillator is to generate a frequency of 800 kHz. The capacitors to be used to have capacitance $C_1 = 100$ pF and $C_2 = 10$pF. Find the value of inductance. (06 Marks)

c. What is frequency stability in oscillators? What factors affect the frequency stability? Explain how crystal oscillator provides good frequency stability. (06 Marks)

8 a. What is a JFET and how does it differ from BJT? Explain the different methods of biasing FET. (07 Marks)

b. Explain the operation of JFET amplifier. Draw the FET small signal model. Calculate the transconductance g_m of a JFET having values of $I_{DSS} = 12$ mA and $V_p = -4$V at bias points i) $V_{GS} = 0$V; ii) $V_{GS} = -1.5$V. (06 Marks)

c. Draw a diagram showing the constructional features of a MOSFET. From the diagram explain in brief how the voltage at the gate controls the flow of carriers. A depletion MOSFET has $I_{DSS} = 12$ mA and $V_P = -4.5$ V. Calculate the drain current at gate source voltages of i) OV; ii) –2V; iii) –3V. (07 Marks)

* * * * *

USN | | | | | | | | | | |

06ES32

Third Semester B.E. Degree Examination, Dec.09/Jan.10
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Describe how diffusion and transition capacitances differ. **(05 Marks)**

b. A full wave bridge rectifier is supplied from the transformer secondary voltage of 100 V. Calculate the dc output voltage and peek inverse voltage of the diodes employed. **(05 Marks)**

c. For the clipper circuit shown in the Fig.1(c), the input is $V_i = 50$ Sin wt. Calculate and plot to scale the transfer characteristic, indicating slopes and intercepts. **(10 Marks)**

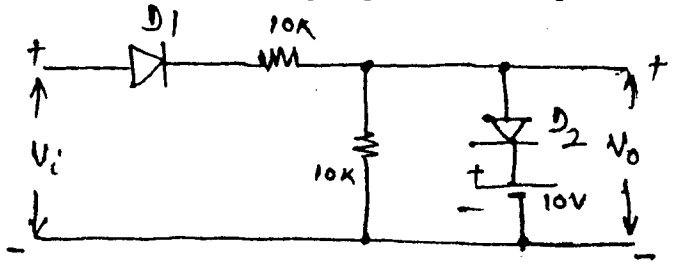


Fig.1(c).

2 a. Determine the voltage V_{eE} and I_c for the voltage divider configuration shown in Fig.2(a). **(10 Marks)**

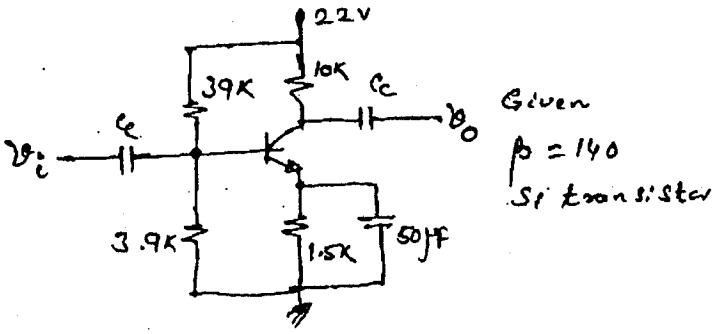


Fig.2(a).

b. Determine R_1 and R_c for the network of Fig.2(b). Given $I_{CQ} = 2$ mA, $V_{CEQ} = 10$ V. Assume S_i transistor. **(10 Marks)**

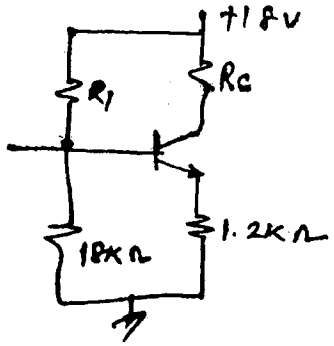
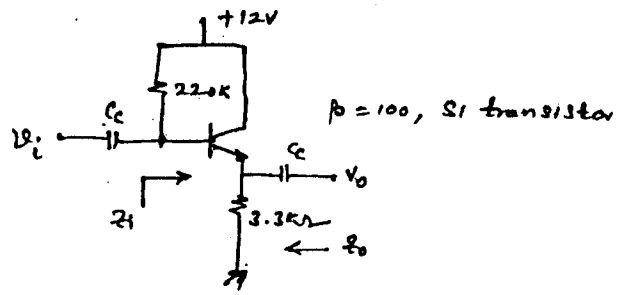


Fig. 2(b)

3 a. For the emtter – follower network of Fig.3(a), using r_e model determine: i) r_e ; ii) z_i ; iii) z_o ; iv) A_V ; v) A_I. (10 Marks)

Fig.3(a).



b. Using complete hybrid equivalent model for a two part system derive expressions for A_i, A_V, z_i and z_o. (10 Marks)

4 a. Prove that Miller effect capacitance $C_{Mi} = (1 - A_v)\, c_f$ and $C_{Mo} = \left(1 - \frac{1}{A_V}\right) c_f$. (10 Marks)

b. A four stage amplifier has a lower 3 db frequency for an individual stage of $f_1 = 40$ Hz and individual upper 3 db frequency of $f_2 = 2.5$ MHz. Calculate the overall lower 3 db and upper 3 db frequency of this full amplifier. Derive the expressions used. (10 Ma

PART – B

5 a. Explain with the help of circuits what is cascade connection and cascode connection. What are the advantages of these connections? (10 Marks)

b. Explain the important advantages of a negative feedback amplifier. (04 Marks)

c. List the four types of feedback connections. Show one practical circuit for each feedback connection. (06 Marks)

6 a. Explain the working of a transformer coupled class B push pull amplifier. (10 Marks)

b. A Class B amplifier provides a 20 V peak signal to a 16 ohm load and a power supply of $V_{cc} = 30$ V. Determine the input power, output power and circuit efficiency. (05 Marks)

c. Calculate the harmonic distortion components for an output signal, having a fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V and fourth harmonic amplitude of 0.05 V. Also calculate the total harmonic distortion. (05 Marks)

7 a. Explain Barkhausen criterion for oscillations. (05 Mar

b. With the help of a need circuit diagram, explain the working of Hartley oscillator. (07 Ma...s)

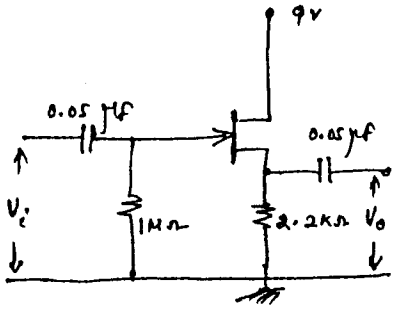
c. List the advantages of a crystal oscillator. Explain the working of a series resonant crystal oscillator. (08 Marks)

8 a. List three advantages of PET over BJT. (03 Marks)

b. With a neat circuit diagram, explain potential divider biasing of JFET. (07 Marks)

c. Calculate the voltage gain and input and output impedance for the circuit of Fig.8(c). (10 Marks)

Fig.8(c).



Given:
$I_{DSS} = 16$ mA
$V_p = -4$V
$r_d = 40$ K Ω
$V_{GSQ} = -2.86$ V.

* * * * *

USN | | | | | | | | | | |

06ES32

Third Semester B.E. Degree Examination, May/June 2010
Analog Electronics Circuit

Time: 3 hrs. Max. Marks:100

Note: ***1. Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. Draw equivalent circuit wherever necessary.

PART – A

1 a. Explain the different diode equivalent circuits – with necessary approximations if any. **(06 Marks)**

b. Define clipper circuit. Draw and explain symmetrical double ended diode clipper circuit with the help of transfer characteristics. **(06 Marks)**

c. A full wave rectifier using centre tapped transformer supplies a resistive load of 1 K Ω. The transformer secondary end to end voltage is 60 V rms at 50 Hz. The filer capacitance is 500 μF. Calculate : i) Ripple factor ; ii) Output resistance of the filter (Ro) ; iii) Vdc ; iv) Idc ; v) % regulation. **(08 Marks)**

2 a. Explain Emitter bias circuit, with the help of B.E. loop and C.E. loop. Write the necessary equations. **(08 Marks)**

b. Explain the circuit of a transistor switch being used as an inverter. **(05 Marks)**

c. Determine the dc bias voltage V_{CE} and the current I_C for the voltage – divider configuration of Fig.2(c), show below. **(07 Marks)**

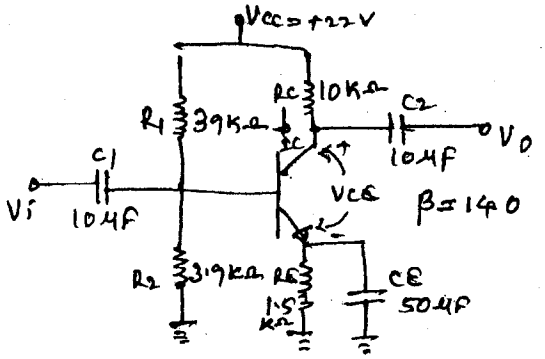


Fig.2(c).

3 a. Define h – parameters. Draw the complete hybrid equivalent circuit of a transistor. **(05 Marks)**

b. Sketch the r_e – equivalent circuit of CE fixed bias configuration and derive the expression for Ar, Ai, Zi and Zo. Show the phase relationship between input and output wave form. **(10 Marks)**

c. For common base configuration shown in Fig.3(c). Determine :
i) re ; ii) Zi ; iii) Zo ; iv) Ar ; v) Ai. **(05 Marks)**

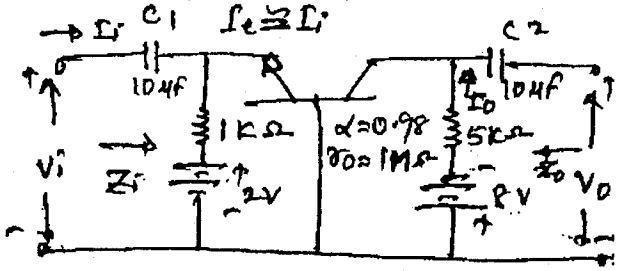


Fig.3(c)

4 a. Describe miller effect and derive an equation for miller input and output capacitances. (10 Marks)

b. Discuss the low frequency response of BJT amplifier and give expression for lower cut-off frequency due to C_C, C_E and C_S. (10 Marks)

PART – B

5 a. Draw the cascade configuration and list the advantages of this circuit. (05 Marks)

b. With necessary equivalent circuit diagram obtain the expression for Zin, Zo and Av for a Darlington Emitter follower. (08 Marks)

c. Derive expression for Zif and Zof for voltage series feed back amplifier and list the advantages of negative feed back amplifier. (07 Marks)

6 a. Give the definition of power amplifiers and list the types of power amplifier based on the location of 2 – point. (04 Marks)

b. Explain the workings of class – B push pull amplifier. Obtain an expression for maximum conversion efficiency of this amplifier. (10 Marks)

c. Calculate the harmonic-distoration components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25, third harmonic amplitude of 0.1 V and fourth harmonic amplitude of 0.05 V and also calculate the total harmonic distoration for the amplitude components given above. (06 Marks)

7 a. Explain how a feed back circuit can be used as oscillators. (04 Marks)

b. Explain with help of circuit diagram, the working of an RC phase shift oscillator. (08 Marks)

c. A quartz crystal has L = 0.12 H, C = 0.04 pF, Cm = 1 pF and R = 9.2 K Ω. Find:
i) Series resonant frequency ; ii) Parallel resonant frequency. (08 Marks)

8 a. Discuss the difference between FET and BJT. (04 Marks)

b. With a necessary oc equivalent model of JFET common-drain configuration. Obtain the expression for Zi, Zo and Av. (10 Marks)

c. Explain FET small signal model with help of graphical representation of gm. (06 Marks)

* * * * *